What is claimed is:

1. An integrated circuit testing apparatus, comprising:

a first test circuit operable to produce a first signal for determining at least one of an operating reference signal of said integrated circuit and a substrate coupling effect on a plurality of components within said integrated circuit;

a second test circuit operable to produce a second signal for determining at least one of a cross-talk effect on said plurality of components and the accuracy of an interconnect capacitance extraction value;

a third test circuit operable to produce a third signal for determining at least one of an effect of system noise on the operational speed of said plurality of components and a maximum degradation expected for a logic path within said integrated circuit; and

a fourth test circuit operable to produce a fourth signal for determining an effect of power supply noise on a signal propagation delay within said integrated circuit.

2. The apparatus of claim 1 wherein said first test circuit further comprises a first ring oscillator, said first ring oscillator being routed to mimic a data path within said integrated circuit and being powered by an external power supply.

3. The apparatus of claim 1 wherein said second test circuit further comprises a second ring oscillator, said second ring oscillator being routed within a core logic area of said integrated circuit and being powered by an external power supply.

4. The apparatus of claim 1 wherein said third test circuit further comprises a third ring oscillator, said third ring oscillator being randomly located within a core logic area of said integrated circuit and being powered by an external power supply.

5. The apparatus of claim 1 wherein said fourth test circuit further comprises a fourth ring oscillator, said fourth ring oscillator being routed to mimic a data path within said integrated circuit and sharing a power supply with a core logic area of said integrated circuit.

6. An apparatus for dynamically testing an integrated circuit, said integrated circuit having a core logic area with a plurality of components therein, the apparatus comprising:

a first test circuit having a first plurality of elements connected by a first plurality of traces, said first plurality of elements and said first plurality of traces routed to mimic a data path within said integrated circuit;

a second test circuit having a second plurality of elements connected by a second plurality of traces, said second plurality of traces being routed within said core logic area;

a third test circuit having a third plurality of elements connected by a third plurality of traces, said third plurality of elements being randomly located within said core logic area; and

a fourth test circuit having a fourth plurality of elements connected by a fourth plurality of traces, said fourth plurality of elements and said fourth plurality of traces routed to mimic a data path within said integrated circuit.

7. The apparatus of claim 6 wherein said first test circuit is operable to produce a first signal used to determine at least one of an operating reference signal for said integrated circuit and a substrate coupling effect on said plurality of components.

8. The apparatus of claim 6 wherein the second test circuit is operable to produce a second signal used to determine at least one of a cross-talk effect on said plurality of components and the accuracy of an interconnect capacitance extraction value.

9. The apparatus of claim 6 wherein said third test circuit is operable to produce a third signal used to determine at least one of an effect of system noise on the operational speed of said plurality of components and a maximum degradation expected for a logic path within said core logic area.

10. The apparatus of claim 6 wherein the fourth test circuit is operable to produce a fourth signal used to determine an effect of power supply noise on a signal propagation delay within said core logic area.

11. The apparatus of claim 6 wherein said first test circuit, said second test circuit, said third test circuit, and said fourth test circuit are ring oscillators.

12. The apparatus of claim 11 wherein said first plurality of elements, said second plurality of elements, said third plurality of elements, and said fourth plurality of elements include at least one of an inverter, a logic gate, and a divider.

13. The apparatus of claim 6 wherein said first test circuit, said second test circuit, and said third test circuit are powered by an external power supply.

14. The apparatus of claim 6 wherein the fourth test circuit shares a power supply with at least one of said plurality of components within said core logic area.

15. The apparatus of claim 6 wherein said first test circuit is located within a reserved area of said integrated circuit.

16. The apparatus of claim 6 wherein at least one of said second plurality of elements is located within a reserved area of said integrated circuit.

17. The apparatus of claim 6 wherein said fourth test circuit is located within a reserved area of said integrated circuit.

18. An integrated circuit, comprising:

a core logic area having a plurality of components therein;

a first test circuit constructed to mimic a data path within said core logic area;

a second test circuit constructed with a plurality of traces routed within said core logic area;

a third test circuit constructed with a plurality of elements randomly placed within said core logic area; and

a fourth test circuit constructed to mimic a data path within said core logic area, said fourth test circuit sharing a power source with at least one of said plurality of components within said core logic area.

19. The integrated circuit of claim 18 wherein said first test circuit is operable to produce a first signal for determining at least one of an operating reference signal of said integrated circuit and a substrate coupling effect on said plurality of components.

20. The integrated circuit of claim 18 wherein said second test circuit is operable to produce a second signal used for determining at least one of a cross-talk effect on said plurality of components and the accuracy of an interconnect capacitance extraction value.

21. The integrated circuit of claim 18 wherein said third test circuit is operable to produce a third signal used to determine at least one of an effect of system noise on the operational speed of said plurality of components and a maximum degradation expected for a logic path within said integrated circuit.

22. The integrated circuit of claim 18 wherein said fourth test circuit is operable to produce a fourth signal used to determine an effect of power supply noise on a signal propagation delay within said integrated circuit.

23. The integrated circuit of claim 18 wherein said first test circuit further comprises a plurality of elements connected by a plurality of traces, said plurality of traces being as short as possible.

24. The integrated circuit of claim 18 wherein the plurality of traces of said second test circuit are routed to test a specific component within said core logic area.

25. The integrated circuit of claim 18 wherein said first test circuit, said second test circuit, and said third test circuit receive power from an external power supply.

26. The integrated circuit of claim 18 wherein said integrated circuit includes a memory device.

27. A combination, comprising:
an integrated circuit; and
a testing system comprising:
a signal generator;
a plurality of ring oscillators responsive to said signal generator; and
a signal analyzer responsive to said plurality of ring oscillators for dynamically measuring the effects of noise and cross-talk on said integrated circuit.

28. The combination of claim 27 wherein said integrated circuit further comprises a core logic area and a reserved area, said core logic area having a plurality of components located therein, said reserved area having a plurality of peripheral circuits located therein.

29. The combination of claim 28 wherein said plurality of ring oscillators includes a first ring oscillator constructed to mimic a data path within said integrated circuit, a second ring oscillator constructed with traces routed within said core logic area, a third ring oscillator randomly placed within said core logic area, and a fourth ring oscillator constructed to mimic a data path within said integrated circuit, said fourth ring oscillator sharing a power source with at least one of said plurality of components within said core logic area.

30. The combination of claim 27 wherein said signal generator is operable to produce at least one of a 'clr' signal and a 'run' signal.

31. The combination of claim 27 wherein at least one of said 'clr' signal and said 'run' signal are applied to at least one of said plurality of ring oscillators.

32. The combination of claim 27 wherein said testing system is operable to determine at least one of an operating reference signal of said integrated circuit, a substrate coupling effect on said integrated circuit, a cross-talk effect on said integrated circuit, the accuracy of an interconnect capacitance extraction value, an effect of system noise on the operational speed of said integrated circuit, a maximum degradation expected for a logic path within said integrated circuit, and an effect of power supply noise on a signal propagation delay within said integrated circuit.

33. The combination of claim 27 wherein said integrated circuit includes a memory device.

34. A method for dynamically testing the effects of signal noise and cross-talk on an integrated circuit having a core logic area, the method comprising:

measuring an inactive operating frequency for each of a plurality of test circuits;

measuring an active operating frequency for each of a plurality of test circuits; and

analyzing said plurality of inactive operating frequencies and said plurality of active operating frequencies to determine the effects of signal noise and cross-talk on said integrated circuit.

35. The method of claim 34 wherein measuring said inactive operating frequency for each of a plurality of test circuits step further comprises:

deactivating said integrated circuit;

counting the number of oscillations of a first test circuit having a first ring oscillator, said first ring oscillator constructed to mimic a data path within said integrated circuit;

counting the number of oscillations of a second test circuit having a second ring oscillator constructed to have traces routed within said core logic area;

counting the number of oscillations of a third test circuit having a third ring oscillator constructed to have plurality of cells randomly located within said core logic area; and

counting the number of oscillations of a fourth test circuit having a fourth ring oscillator, constructed to mimic a data path within said integrated circuit, said fourth ring oscillator sharing a power source with said core logic area.

36. The method of claim 34 wherein measuring said active operating frequency for each of a plurality of test circuits step further comprises:

activating said integrated circuit;

counting the number of oscillations of a first test circuit having a first ring oscillator, said first ring oscillator constructed to mimic a data path within said integrated circuit;

counting the number of oscillations of a second test circuit having a second ring oscillator constructed to have traces routed within said core logic area;

counting the number of oscillations of a third test circuit having a third ring oscillator constructed to have plurality of cells randomly located within said core logic area; and

counting the number of oscillations of a fourth test circuit having a fourth ring oscillator, constructed to mimic a data path within said integrated circuit, said fourth ring oscillator sharing a power source with said core logic area.

37. The method of claim 34 wherein said analyzing step further comprises at least one of:

comparing an inactive oscillation count of a second test circuit to an operating reference signal to determine the accuracy of an interconnect capacitance extraction value, said operating reference signal being equal to an inactive oscillation count of a first test circuit;

comparing an inactive oscillation count of a third test circuit to said operating reference signal to determine a maximum degradation for a logic path within said integrated circuit;

comparing an inactive oscillation count of a fourth test circuit to said operating reference signal to determine an effect of power supply noise on a propagation delay within said integrated circuit;

comparing an active oscillation count of said first test circuit to said operating reference signal to determine an effect of substrate-noise-coupling on said integrated circuit;

comparing an active oscillation count of said second test circuit to said inactive oscillation count of said second circuit to determine an effect of cross-talk on a delay of said integrated circuit; and

comparing an active oscillation count of said third test circuit to said inactive oscillation count of said third circuit to determine an effect of system noise on an operational speed of said integrated circuit.

38. A method comprising:

measuring an inactive operating frequency of a first test circuit, said first test circuit having a first plurality of elements connected by a first plurality of traces, said first test circuit being constructed to mimic a data path within said core logic area, said inactive operating frequency representing an operating reference signal;

measuring an inactive operating frequency of a second test circuit, said second test circuit having a second plurality of elements connected by a second plurality of traces, said second plurality of traces being routed within said core logic area;

measuring an inactive operating frequency of a third test circuit, said third test circuit having a third plurality of elements connected by a third plurality of traces, said third plurality of elements being randomly located within said core logic area; and

measuring an inactive operating frequency of a fourth test circuit, said fourth test circuit having a fourth plurality of elements connected by a fourth plurality of traces, said fourth test circuit being constructed to mimic a data path within said core logic area, said fourth test circuit sharing a power source with at least one of said plurality of components within said core logic area.

39. The method of claim 38 further comprising:

determining the accuracy of an interconnect capacitance extraction value by comparing said inactive operating frequency of said second test circuit to said operating reference signal.

40. The method of claim 38 further comprising:

determining a maximum degradation for a logic path within said integrated circuit by comparing the inactive operating frequency of said third test circuit to said operating reference signal.

41. The method of claim 38 further comprising:

determining an effect of power supply noise on a propagation delay within said integrated circuit by comparing the inactive operating frequency of said fourth test circuit to said operating reference signal.

42. The method of claim 38 further comprising:

measuring an active operating frequency of said first test circuit;

measuring an active operating frequency of said second test circuit;

measuring an active operating frequency of said third test circuit; and

measuring an active operating frequency of said fourth test circuit.

43. The method of claim 42 further comprising:

determining an effect of substrate-noise-coupling on said integrated circuit by comparing the active operating frequency of said first test circuit to said operating reference signal.

44. The method of claim 42 further comprising:

determining an effect of cross-talk on a delay within said integrated circuit by comparing the active operating frequency of said second test circuit to the inactive operating frequency of said second circuit.

45. The method of claim 42 further comprising:

determining an effect of system noise on an operational speed of said integrated circuit by comparing the active operating frequency of said third test circuit to the inactive operating frequency of said third circuit.

46. The method of claim 42 wherein said first test circuit includes a first ring oscillator, said first ring oscillator having at least one of a logic gate and an inverter, wherein the step of measuring an inactive operating frequency of a first test circuit and the step of measuring an active operating frequency of a first test circuit further comprise:

resetting a divider;

activating said first ring oscillator, an output of said activated first ring oscillator changing states;

counting the number of times said activated first ring oscillator changes states with said divider; and

deactivating the ring oscillator after a first predetermined time period has expired.

47. The method of claim 42 wherein said second test circuit includes a second ring oscillator, said second ring oscillator having at least one of a logic gate and an inverter, wherein the step of measuring inactive operating frequency of a second test circuit and the step of measuring an active operating frequency of a second test circuit further comprise:

resetting a divider;

activating said second ring oscillator, an output of said activated second ring oscillator changing states;

counting the number of times said activated second ring oscillator changes states with said divider; and

deactivating the second ring oscillator after a second predetermined time period has expired; and

48. The method of claim 42 wherein said third test circuit includes a third ring oscillator, said third ring oscillator having at least one of a logic gate and an inverter, wherein the step of measuring inactive operating frequency of a third test circuit and the step of measuring an active operating frequency of a third test circuit further comprise:

resetting a divider;

activating said third ring oscillator, an output of said activated third ring oscillator changing states;

counting the number of times said activated third ring oscillator changes states with said divider; and

deactivating the third ring oscillator after a third predetermined time period has expired.

49. The method of claim 42 wherein said fourth test circuit includes a fourth ring oscillator, said fourth ring oscillator having at least one of a logic gate, an inverter and a divider, wherein the step of measuring inactive operating frequency of a fourth test circuit and the step of measuring an active operating frequency of a fourth test circuit further comprise:

resetting a divider;

activating said fourth ring oscillator, an output of said activated fourth ring oscillator changing states;

counting the number of times said activated fourth ring oscillator changes states with said divider; and

deactivating the fourth ring oscillator after a fourth predetermined time period has expired.

50. The method of claims 46, 47, 48, and 49 wherein said first, second, third, and fourth predetermined time periods are equal.

51. An integrated circuit testing apparatus, comprising at least two of the following circuits:

a first test circuit operable to produce a first signal for determining at least one of an operating reference signal and a substrate coupling effect on a plurality of components within an integrated circuit;

a second test circuit operable to produce a second signal for determining at least one of a cross-talk effect on said plurality of components and the accuracy of an interconnect capacitance extraction value;

a third test circuit operable to produce a third signal for determining at least one of an effect of system noise on the operational speed of said plurality of components and a maximum degradation expected for a logic path between said plurality of components; and

a fourth test circuit operable to produce a fourth signal for determining an effect of power supply noise on a signal propagation delay within said plurality of components.